



Effect of Annealing Temperature to the Electrical and Photovoltaic Properties of a Two-Dimensional WSe₂/MoS₂ P-N Heterojunction

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Abstract

Starting from the advent of graphene, Two-Dimensional (2D) materials have been studied by many researchers for their unique characteristics and great potential to be utilized in various applications. Transition Metal Dichalcogenides (TMDs) are family of 2D materials which have been evaluated as more promising materials than graphene, in that they have sizable energy band gaps. Especially, TMD semiconductors which are represented by MoS₂ and WSe₂ were getting great attention for their high mobility, flexibility and transparency, which are superior to the conventional bulk semiconductor, Si. In addition, any combination of 2D materials can easily form a VAN DER WAALS (vdW) heterojunction, which exhibits excellent interface quality. Therefore the potential of 2D material grows even bigger. In this study, we have fabricated a 2D WSe₂/MoS₂ p-n heterojunction device and evaluated the effect of annealing temperature to it, in terms of its electrical and photovoltaic properties. A WSe₂/MoS₂ p-n heterojunction showed clear current rectification as a p-n diode, and also operated well as a photovoltaic cell under white light. After conducting vacuum annealing under various temperature conditions to the as-fabricated devices, both the electrical and photovoltaic characteristics have changed in a great extent. The electrical property change was evaluated by means of diode ideality factors and the photovoltaic performance was analyzed by comparing the photovoltaic parameter changes.

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Introduction

2D material, which is best known for graphene, is a crystalline material consisted of a layered structure. In contrast to the strongly covalent-bonded atoms within the single layer, inter-layer connection is very weak, formed by vdW interactions. As a result, 2D materials can be easily separated into the extremely thin atomic layers even by mechanical exfoliation, and those layers possess unique characteristics differ from the bulk materials [1-3]. Recently, TMD materials which are composed of one transition metal (M) atom and two chalcogen (X) atoms in MX₂ form are getting great attention as one of the most useful 2D materials in various fields. Unlike graphene, TMDs have a sizable band gap, so their applications became more diverse than graphene. Started from the field-effect transistor [4,5], the usage of TMD semiconductors was expanded to a logic device [6,7], a photo detector [8,9], a gas sensor [10,11], a memory device [12,13] and even a solar cell [14,15].

Unlike conventional bulk semiconductors which are connected by covalent bonding, any combination of different 2D materials can easily form a vdW heterojunction which is free of lattice mismatch problems [16]. By simply stacking different atomic layers, a heterostructure with superior interface quality can be achieved. Such special characteristic of 2D materials makes them more promising and also enables various applications based on p-n junction [17-19].

Here, we have fabricated a TMD p-n heterojunction device, by utilizing WSe₂ and MoS₂ as p-type and n-type semiconductors. Both WSe₂ and MoS₂ are one of the most well-known TMD semiconductors due to their high performance. Although there are several reports showing the basic properties of a WSe₂/MoS₂ p-n junction [15,17,20], deep research in terms of the factors and mechanisms of the performance improvement is not sufficient. Therefore, we not only show the electrical and photovoltaic characteristics of the WSe₂/MoS₂ p-n heterojunction device, but also discuss on the effect of annealing temperature to its performance enhancement.

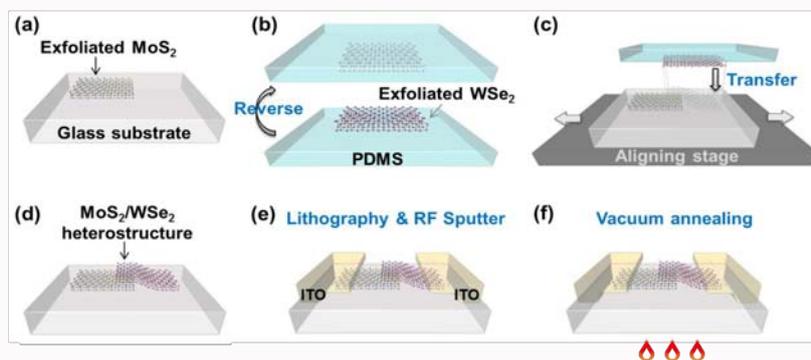


Figure 1: Process flow for fabricating the $\text{WSe}_2/\text{MoS}_2$ p-n heterojunction device in this paper. (a) Exfoliation of MoS_2 onto the substrate. (b) Exfoliation of WSe_2 onto the PDMS stamp. (c) Transfer process to build a heterojunction. (d) A $\text{MoS}_2/\text{WSe}_2$ heterostructure on the substrate. (e) Patterning RF sputtered ITO electrode by lift-off. (f) Annealing the samples inside a vacuum chamber.

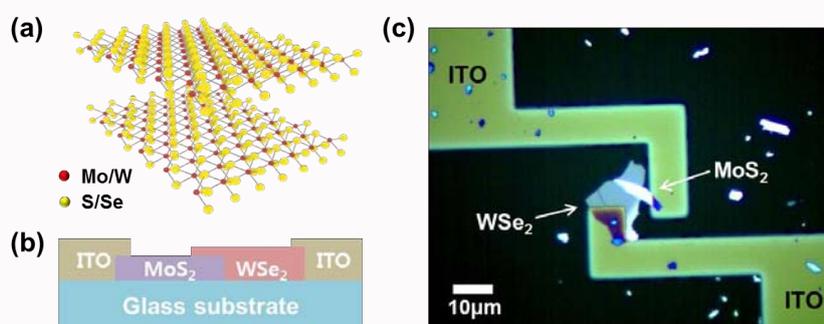


Figure 2: (a) Crystal structure of 2D MoS_2 and WSe_2 atomic layers. (b) Schematic image on the cross-section of the $\text{WSe}_2/\text{MoS}_2$ p-n heterojunction device. (c) Optical microscope image of the real sample.

Materials and Methods

For this study, commercial bulk crystals of WSe_2 (2D Semiconductors) and MoS_2 (SPI Supplies) were utilized for the semiconducting layers and alkali-free glass of Eagle 2,000 (Corning) was used for the substrate. Figure 1 exhibits the whole fabrication process of our 2D $\text{WSe}_2/\text{MoS}_2$ p-n heterojunction devices. By mechanical exfoliation method using adhesive tape, multi-layer of MoS_2 was first transferred onto the glass substrate and WSe_2 was transferred onto the Polydimethylsiloxane (PDMS) stamp. Under the optical microscope, both 2D flakes with adequate thickness and size were selected and aligned by utilizing aligning stage and micromanipulator. By dry transfer process [21], a $\text{WSe}_2/\text{MoS}_2$ heterostructure was formed and ITO electrodes were connected to the each side, by conventional lithography, RF sputtering and lift-off process. Finally, the samples were annealed inside a vacuum hot plate for 1 hr, under various temperature conditions. For device characterization, Keithley 4,200 parameter analyzer was utilized.

Results and Discussion

Figure 2a shows a crystal structure of MoS_2 and WSe_2 atomic layers, which are consisted of metal atoms (Mo or W) sandwiched by chalcogen atoms (S or Se). From Figure 2b and 2c, the structure of our 2D $\text{WSe}_2/\text{MoS}_2$ p-n heterojunction device can be identified. MoS_2 and WSe_2 flakes are stacked in series with overlap and each side of the heterostructure is connected to the ITO electrodes. As a result, the carrier extraction from the junction area to the electrode occurs in a lateral direction. The junction area was defined as the overlapped region of two different semiconductors, which corresponds to 17.51

μm^2 for the sample shown in Figure 2c. However, the junction area varies in size within $10 \mu\text{m}^2$ to $30 \mu\text{m}^2$ range by each sample.

Right after the device fabrication, samples were annealed under vacuum atmosphere for 1 hour. At first, the samples were annealed at 130°C and its electrical property was measured inside a vacuum chamber. Then, the same sample was annealed at higher temperature and was followed by the electrical characteristic measurement. Such experimental process of annealing and measuring was repeated until the annealing temperature has reached 200°C . Figure 3 is the result of electrical property observation under various conditions of annealing. The $\text{WSe}_2/\text{MoS}_2$ p-n heterojunction showed a clear current rectification under voltage bias sweep from negative to positive region. It can be concluded that a p-n junction has formed successfully by stacking 2D semiconductors and also operate well as a p-n diode. In terms of annealing temperature, the on-current level at positive voltage bias tends to increase as the temperature gets higher until 190°C . However, after exposed to 200°C anneal, the positive current of the device has decreased than before. As the inset of Figure 3a shows, the steepness of the I-V curves under low positive bias region changes in similar ways with the on-current with respect to the annealing temperature.

In order to observe the annealing effect to the I-V characteristics of the 2D p-n heterojunction in detail, change in diode ideality factor (n) was analyzed. Based on the Shockley diode model, diode ideality factor can be calculated from the linear fitting of $\ln(I)$ -V plot, where $n = (1/\text{slope}) (q/kT)$. I-V curve of 130°C annealed sample was too far from the ideal diode curve to introduce linear fitting and extract reliable n value. Therefore, ideality factor of p-n diodes with 150°C ,

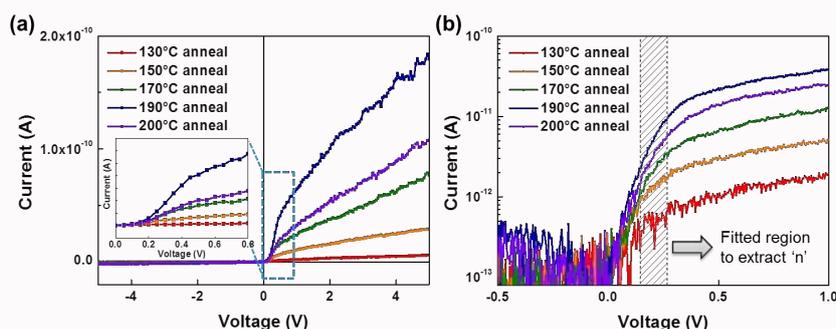


Figure 3: (a) Linear I-V characteristics of the $\text{WSe}_2/\text{MoS}_2$ heterojunction device after annealing under various temperatures. Inset magnifies the I-V curves under low applied voltage range of 0 to 0.8V (b) Semi-log plot of I-V curves for extracting diode ideality factors (n).

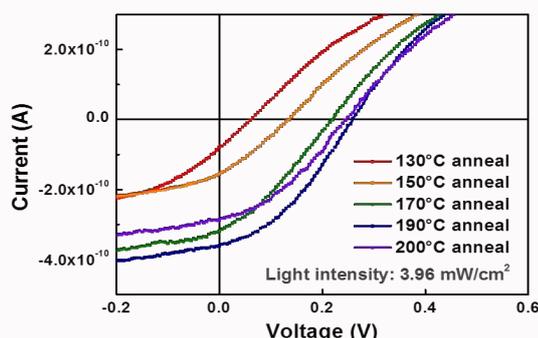


Figure 4: I-V characteristics of a $\text{WSe}_2/\text{MoS}_2$ p-n heterojunction under various annealing temperatures, which were measured under the white light with intensity of 3.96 mW/cm^2 .

170°C, 190°C and 200°C annealing were compared, whose n value turned out to be 6.39, 4.03, 3.13 and 3.59 respectively. Similar to the trend of on-current change, a $\text{WSe}_2/\text{MoS}_2$ p-n junction showed gradual improvement in its diode performance until 190°C and started degradation from 200°C.

The photovoltaic performance of our 2D p-n heterojunction was also observed while applying various annealing temperatures. Halogen lamp was utilized for the irradiation source and the light was shined onto the active region of our device during measurement. Figure 4 exhibits I-V plots measured under white light. It shows that the $\text{WSe}_2/\text{MoS}_2$ p-n heterojunction operate as a photovoltaic device with sizable Short-Circuit Current (ISC) and Open-Circuit Voltage (VOC). It can be found that the annealing temperature affects photovoltaic performance in great extent. Table 1 is a list of photovoltaic parameters which are extracted from the I-V curves of Figure 4. All the parameters were improved along with the increase of annealing temperature up to 190°C, but started to degrade after exposed to 200°C. Accordingly, our $\text{WSe}_2/\text{MoS}_2$ p-n photovoltaic device showed maximum efficiency of ~5% after 1 hr annealing under 190°C.

During annealing process, several kinds of change occur simultaneously in each part of the device. There are unwanted residues on the surface of the sample which are introduced by adhesive tape during the exfoliation process or photoresist used in lithography. Such residues, which are known to hinder the current flow, can be decomposed under high temperature. In case of ITO, which was utilized as an electrode of our heterojunction device, its sheet resistance tends to decrease when it goes through a vacuum annealing process in sufficiently high temperature [22]. Furthermore, even 2D materials

Table 1: Photovoltaic parameters of the $\text{WSe}_2/\text{MoS}_2$ p-n heterojunction after annealing under various temperatures.

Annealing Temp.	130°C	150°C	170°C	190°C	200°C
J_{sc} (mA/cm^2)	0.45	0.89	1.82	2.06	1.63
V_{oc} (V)	0.06	0.135	0.22	0.26	0.245
FF%	27	29	31	37	36
PCE (%)	0.19	0.87	3.09	4.96	3.65

have small amount of dangling bonds introduced by defects and it is known that annealing process can cure those sites and adjust the Stoichiometry properly [23-24]. Electrical and photovoltaic property enhancement with the increase of the annealing temperature seems to be originated from all those phenomena. The degradation which has appeared at very high post-anneal temperature might be caused by the composition change of the TMDs or interface trap density change [25-26].

Conclusion

In this study, we have demonstrated the electrical and photovoltaic characteristics of a $2\text{DWSe}_2/\text{MoS}_2$ p-n heterojunction device and also the influence of annealing temperature to those performances. Contributed by the advantages that 2D materials possess, simply stacked multi-layers of p-type and n-type TMD semiconductors have shown clear p-n diode property and also photovoltaic effect with power conversion efficiency of ~5% after annealing. The effect of annealing temperature was systematically observed and turned out to improve the device performance in great extent. This result exhibits the promising future of 2D materials to be utilized in various applications.

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